CLAIMS

1. A Packet Processor for a communication apparatus, for processing received and transmitted data streams made of packets, each packet mainly comprises a header and a payload section, comprising:

(A) A receiving part comprising:

(a) A receiving PHY interface by which a flow of data stream is conveyed from a Modulator-Demodulator section of a modem to the Packet Processor;

(b) A receiving Tubular Bus receiving the said flow of data stream which is conveyed from the Modulator-Demodulator section of the modem to the Packet Processor, said receiving Tubular Bus conveying data, while processed, in the direction from the said receiving PHY interface to a host interface;

(c) At least one processing unit between sections of the said first Tubular Bus for sequentially receiving portions of a data stream from a section of the Tubular Bus, processing the same, and outputting the processed data to a next section of the said first Tubular Bus;

(d) One FIFO storage unit before and one FIFO storage unit after any of the said processing units on the receiving Tubular Bus, for providing a temporary storage for portions of the data stream; and

(e) A first host interface for receiving data from the receiving Tubular Bus and conveying it to a host.

(B) A transmitting part comprising:

(f) A second host interface for receiving data from the host and conveying it to a second Tubular Bus;

(g) A transmitting Tubular Bus for receiving the said flow of data stream which is conveyed from the host to the Packet Processor, said transmitting Tubular Bus conveying the data stream, while processed, in the direction from the said second host interface to a transmitting PHY interface;

(h) At least one processing unit between sections of the said transmitting Tubular Bus, for sequentially receiving portions of the data stream from a section of the Tubular Bus, processing the same, and outputting the processed data to the next section of the said transmitting Tubular Bus;

(i) One FIFO storage unit before and one FIFO storage unit after any of the said processing units on the second Tubular Bus, for providing a temporary storage for portions of the data stream; and

(j) A transmitting PHY interface for receiving processed data from the transmitting Tubular Bus and conveying the same to a Modulator-Demodulator section.

(C) A Backbone Bus for conveying management data, instructions, and addresses between various components of the Packet Processor;

and

(D) Timing and control means for administering the operation of the Packet Processor, and particularly the timing of using transmission slots for the transmit path.

2. A Packet Processor according to claim 1, wherein each one of the processing units in the module functions independently, but simultaneously, with the other processing units of the module.

3. A Packet Processor according to claim 1, comprising two processing units in the receiving part and two processing units in the transmitting part.

4. A Packet Processor according to claim 3, wherein, in the receiving part, the processing unit closer to the demodulator handles the tasks of mainly processing the header, deframing the data stream, and detecting and correcting errors in the header of the received data stream. The processing unit closer to the host, mainly handles the tasks of logical analysis, including determining the length and type of the packets (management, or data), possible concatenation of packets, decrypting the received data stream, and error detecting and correcting of the data portion of the data stream. In the transmitting part, the processing unit closer to the host mainly handles the task of controlling allocation, and prioritizing the transmission sequences, and activities related to the creation of the header CRC of the transmitted data stream. The processing unit closer to the modem mainly handles the task of the creation of the main CRC, encription, and framing of the transmitted data.

5. A Packet Processor according to claim 1, wherein each processing unit comprises a processor and at least one co-processor.

6. A Packet Processor according to claim 1, wherein each processing unit also comprises an internal memory.

7. A Packet Processor according to claim 6, wherein the internal memory of each processing unit includes an instruction cache memory and a Scratch Pad RAM.

8. A Packet Processor according to claim 1, further comprising a connection to an external memory unit.

9. A Packet Processor module according to claim 1, wherein the communication with the external memory unit is made by a processing unit of the packet processor, via the Backbone Bus, and an external bus arbiter.

10. A Packet Processor according to claim 1, wherein each of the FIFO units comprises a plurality of memory cells for providing a sequential temporary storage for portions of the data stream.

11. A Packet Processor according to claim 1, further comprising a connection to one or more external devices.

12. A Packet Processor according to claims 11 and 8, wherein one of said devices is a storage unit, containing a code for operating the processor, said code being downloaded into the internal memory of each processing unit of the packet processor, and into said external memory unit when initializing the packet processor.

13. A Packet Processor according to claim 1, further comprising an External Bus for communication of the module with an external memory unit.

14. A Packet Processor according to claim 13, wherein the communication with the external memory unit is made by a processing unit of the packet processor, via the External Bus, and an external bus arbiter.

15. A Packet Processor according to claim 1, further comprising a debugging unit for assisting in the debugging of the packet processor.

16. A Packet Processor module according to claim 1, further comprising a DMA control unit for enabling internal transfer of data blocks between internal components of the packet processor, and transfer of data blocks between internal components of the packet processor and components external to the packet processor.

17. A Packet Processor according to claim 1 fabricated in a VLSI form.

18. A Packet Processor according to claim 1, further comprising a Serial Interface for carrying out communication of the module with external serial components.

19. A Packet Processor according to claim 1, further comprising an Interrupt Central Unit for handling interruptions to components in the module.

20. A Packet Processor according to claim 1 for use in communication apparatus.

21. A Packet Processor according to claim 20, wherein said communication apparatus is a modem.

22. A Packet Processor according to claim 20, wherein said communication apparatus is a modem for TV cables.

23. A Packet Processor according to claim 20, for use as a MAC module for a modem.

24. A Packet Processor according to claim 20, for use in a communication routers.

25. A Packet Processor according to claim 1, wherein each processing unit comprises means for embedding one or more macro-instruction with the data flowing in the tubular bus, said macro instruction flowing with the data over the tubular bus to a destination component downstream the tubular bus, and is used for controlling said component.

26. A Packet Processor according to claim 25 wherein the component in the tubular bus which is the destination of said macro-instruction is a FIFO.

27. A Packet Processor according to claim 1 wherein the second FIFO downstream the receiving bus is further associated with an address filter.

28. A Packet Processor according to claim 27 wherein the said address filter is used for comparing a destination address that is detected in the data stream with a list of addresses stored in said address filter, and according to the result of the comparison, determines whether an operation should be taken or not on at least a portion of the data stream.

29. A Packet Processor according to claim 27 wherein one operation that is taken based on said comparison is a flushing of the content of a FIFO and an ignoring of a portion of the data stream.

30. A Packet Processor according to claim 1 wherein each of the processing units of the transmitting and/or receiving parts is a RISC processor.

31. A Packet Processor according to claim 30 wherein each RISC processor of the transmitting and/or receiving parts is of an ARC type processor.

32. A packet processor according to claim 1, wherein the timing and control means are also used for administering the allocation of timing slots for the transmitted data stream.

33. A Packet Processor according to claim 1 wherein the first and second host interfaces are fabricated within a same interface.

34. A Packet Processor according to claim 1, for use in a modem for a wireless LAN.

35. A Packet Processor according to claim 1, for use in Internet Protocol telephone modems.

36. A Packet Processor according to claim 1 wherein the backbone bus is a ring type bus.

37. A Packet Processor according to claim 1, essentially as described and illustrated.